ABSTRACT OF THE DISCLOSURE

A detecting circuit (REFH, CM11, LA1, TN1, RN1) which detects an overcurrent flowing through a power-MOS transistor (401) in an output stage to output a first signal (ITN1) is disposed in a first driving circuit (303H) on the side of a high-side driver. Another detecting circuit (REFL, CM21, LA2, TN2, RN2) which detects an overcurrent flowing through a power-MOS transistor (402) in the output stage to output a second signal (ITN2) is disposed in a driving circuit (303L) on the side of a low-side driver. The first signal (ITN1) is converted to a third signal (ITT2) based on a negative power supply (VPP-), by a signal converting circuit. The third signal is added to the second signal. In response to the addition signal, a pulse signal to be input to the driving circuits (303H and 303L) is blocked.